Remarks

Original claims 6 - 36 have been canceled. Claims 1-5 and 38 - 81 are presently pending.

Original claims 1-5 have been amended to specify that the linear address information and page frame information in the segment descriptor memory can be used to initiate a tentative memory reference, and without performing a virtual-linear-physical address translation. These features are neither disclosed nor suggested in Crawford '836, nor in any of the references submitted or considered to date. Since this feature is neither disclosed nor suggested by any of the art considered to date, applicant submits that the above claims are allowable at this time.

All of the new claims submitted herewith (38 - 81) are distinguishable over the art as well, since applicants believe they are the first to disclose and generally describe a *fast* physical address generator for use in a virtual-linear-physical address translation environment.

Enclosed also is an IDS for all the material references known to applicant. Most of these references were already considered in the parent application. For those references not considered, (1) EP 0-668-565 (Kranich); (2) U.S. Patent No. 4,400,774 (Toy); and (3) U.S. Patent No. 5,165,028, applicant submits the following explanation of why the present invention distinguishes thereover:

First, the Kranich reference does not make any mention of a combination of segmentation and paging based address translation, or a virtual-linear-physical conversion of any kind. In fact, it seems that a different type of address translation is described because at column 9, ll. 55 - column 10, ll. 35 it discusses a virtual address in the form of a virtual "page" system, which is not a "virtual address" of the segment identifier plus segment offset variety disclosed and claimed in the present invention. See present disclosure at p. 2, ll. 4-15 (discussing segmentation). In Kranich the virtual address is disclosed to already contain the page offset (see c.10, ll. 15-18) and therefore no segmentation (virtual to linear address conversion) operation is ever disclosed to occur. Hence there is no "segment," no "segment identifier," no "segmentation" unit or circuit, no "linear address," etc. etc., as those terms are used in the claims. Moreover, as indicated in the attached supplemental IDS, while Kranich claims a U.S. priority date prior to the present application (and may conceivably become 102(e) art at some point), the above European application was not published until after the filing date of the present invention, and therefore it is not believed to be prior art to the present application at this time. Since its status cannot be confirmed at this time, however, applicant requests that it be considered in the present application.

The Toy reference seems deficient for similar reasons. The Zulian reference also makes

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mention of a logical (virtual) address that has an offset field that is the same as the physical address, see column 3, ll. 55-59, (like the Kranich virtual paging), and this disclosure is similarly different from the virtual addresses used in the present invention. The Toy reference construction of the virtual address also does not result in a virtual - linear - physical address conversion of the type generally described in the present disclosure.

In short, the present invention solves the timing bottleneck created by repetitive virtual-linear-physical address calculations in segmentation plus optional paging address translation systems (such as shown in Crawford '836) by using a tentative memory reference and this concept is neither disclosed nor suggested in any of the above references. Accordingly, the present claims are distinguishable over these newly submitted references as well, and should be allowable.

Should the Examiner believe it is necessary or fruitful to discuss any of the above points in person, Applicant is open to a teleconference (408-342-1862) at any convenient time.

Respectfully submitted,

Law+

Date: August 4, 1997

J. Nicholas Gross, Attorney, Reg. No. 34,175

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 4th of August, 1997.